Design And Implementation of Automatic Washing Machine Using Verilog HDL

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Abstract- *This project proposes to demonstrate the capabilities and scope of Verilog HDL by implementing the control system of an automatic washing machine. This project accomplishes the above mentioned objective by implementing the Control System of an automatic washing using the Finite State Machine model. The Control System generates the control signals to control the overall operation of the washing machine. The Digital Design is simulated using Xilinx 14.7 ISE. As described by digital system the language Verilog HDL is widely used in the circuit design, its own advantages to be able to use software language describe hardware features that makes it has good readability, portability, etc. Its advantages not only reduce the hardware development cycle but also greatly reduce development costs. This article describes the characteristics and application of Verilog HDL and take the automatic washing machine as examples to illustrate the practicality of HDL. The result of simulation shows this method is feasibility and effectiveness.*

Keywords- Xilinx 14.7 ISE, Verilog HDL

I. INTRODUCTION

The main factor is the language syntax - since Verilog is based on C and VHDL is based on ADA.Verilog is easier to learn since C is a far simpler language. It also produces more compact code: easier both to write and to read. Furthermore, the large number of engineers who already know C (compared to those who know ADA) makes learning and training easier. VHDL is very strongly typed, and allows programmer to define their own types although, in practice, the main types used are either the basic types of the language itself, or those defined by the IEEE. The benefit is that type checking is performed by the compiler which can reduce errors; the disadvantage is that changing types must be done explicitly. Verilog has two clear advantages over VHDL It allows switch-level modeling which some designers find useful for exploring new circuits. It ensures that all signals are initialized to "unknown" which ensure s that all designers will produce the necessary logic to initialize their de sign - the base types in VHDL initialize to zero and the "hasty" designer may omit a global reset.

II. PROPOSED METHODOLOGY

The washing machine controller has the following functionalities: 1. The wash machine has the following states: idle, beep lid, beep clothes, beep surf, beep tap, soak, wash, drain, final beep. 2. Different time durations are allocated to each mode of operation using various up counters. 3. Different buzzer sounds for different input faults. The controller is composed of a finite - sate machine (FSM) block and a counter. The FSM block receives some signals from the user, from the timer, and from other hardware parts such as the door sensor. FSM block output control the counter and other hardware components of the washing machine. Table1 identifies the FSM input and output signals and their functionality. The counter generates the correct time periods required for each cycle after it has been reset. The timer block is composed of an up-counter and combinational logic to give the correct time signals once certain count values have been achieved. The timer values will be determined by the clock frequency being used in the system.

IV. WORKING CONTROL SYSTEM

The working of the washing machine control system is described in the flow chart as shown in figure . System flow chart of Washing Machine Controller The FSM has 9 states as shown in figure. State transitions take place according to the timing control signals generated by the counter and inputs given to a particular state. The processing in the next state depends on outputs produced in the previous state.State transitions take place according to the timing control signals generated by the counter and inputs given to a particular state. The processing in the next state depends on outputs produced in the previous state.

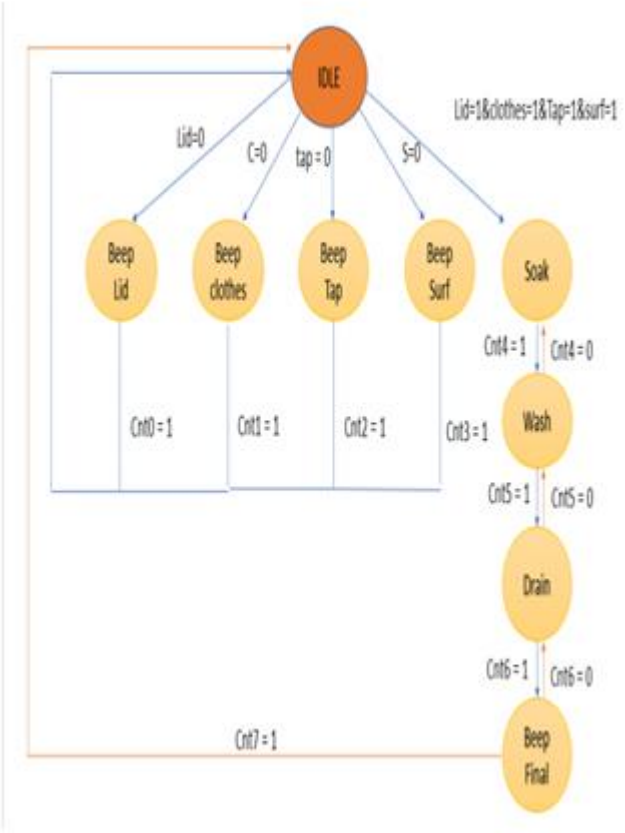

Fig: System State Diagram of Washing Machine Controller

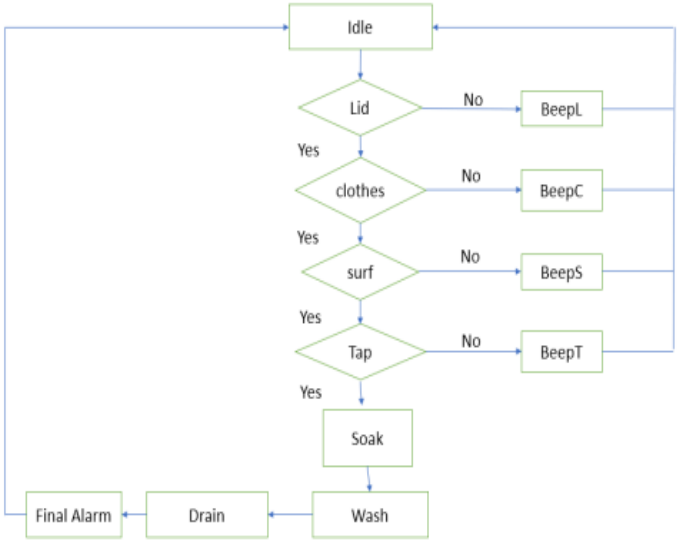

Fig: System flow chart of Washing Machine Controller

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V. RESULT

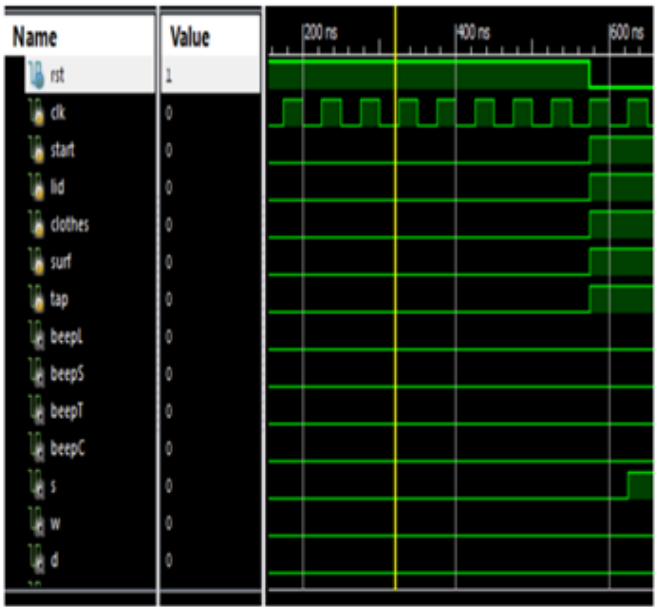

Fig: When Reset (rst) is Active High that is logic 1 then all states is in OFF condition

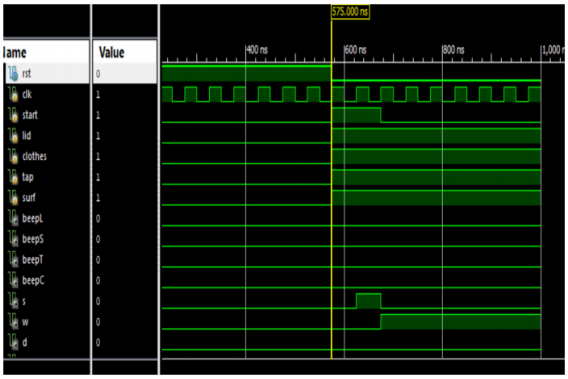

Fig: When Reset (rst) is Active Low that is logic 0 then all states is in ON condition

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